

DSP STAR AD/DA User's Manual

Revision 1.8

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1. Installation

The DSP STAR AD/DA board can be added to the DSP STAR Kit or TI DSK or TI EVM board through expansion connector as shown in Figure 2 and Figure 2, respectively. Make sure the power select switch should be to INT side, so that power to the AD/DA module is given from the underlying DSK board.



Figure 1. Installation of AD/DA with DSP STAR Kit board



Figure 2. Installation of AD/DA with TI DSK board

2. AD/DA Hardware

The DSP STAR AD/DA Module is a high speed Analog-to-Digital and Digital-to-Analog conversion hardware board which can be used as an add-on module to DSP STAR Kit through the expansion connector. Since expansion connection complies to Texas Instrument (TI) Compliant Expansion Connection, TI C6xEVM or TI C6x Starter Kit can also be used with DSP STAR AD/DA module. The module houses four input analog channels of 1.5M 12-bit A/D conversion and two output analog channels of 165M 12-bit D/A conversion. Figure 3 show a real image of AD/DA module and Table 1 shows the key features.

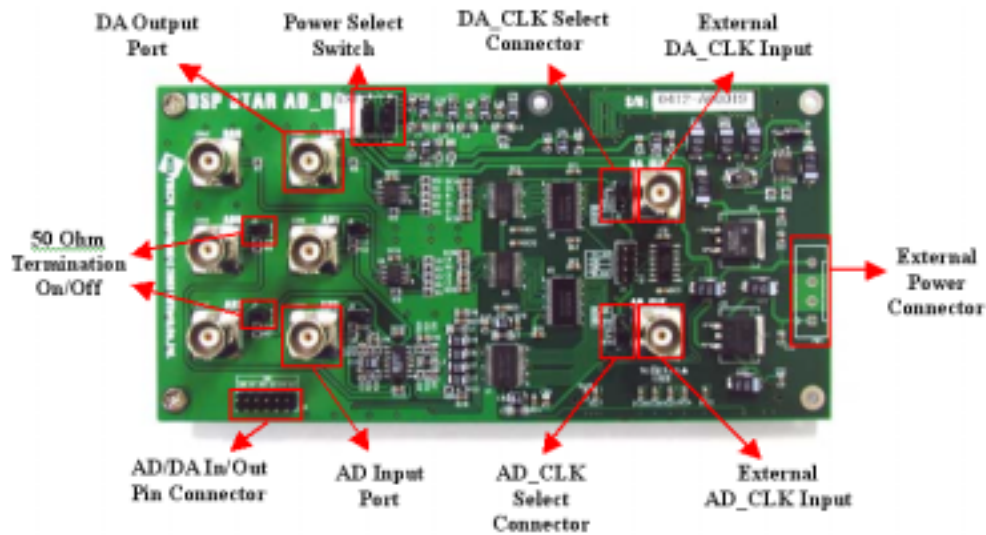


Figure 3. DSP STAR AD/DA Module

Table 1. AD/DA Key Features

ADC	THS1206 12 bit, Up to 6MSPS BNC and PIN connectors
DAC	DAC902 12 bit, Up to 165MSPS BNC and PIN connectors
Clock Source	Internal (Timer Clock)/External External Clock Connector (BNC and PIN)
Power	Internal (DSP Board Power), External Selectable
Bus Expansion	Texas Instrument Expansion Daughter Card Interface

2.1. ADC (Analog to Digital Converter)

The DSP STAR AD/DA module uses the THS1206 chip, of which features are as follows:

- High Speed 6M Samples-per-second ADC
- Four Single Ended Analog Inputs
- 3-V or 5-V Digital Interface Compatible
- 5-V Analog Single Supply Operation
- Glueless DSP Interface
- Parallel Micro processor/DSP Interface
- Integrated FIFO
- Analog Input Range : $\pm 1V$

2.2. DAC (Digital to Analog Converter)

The DSP STAR AD/DA module uses two DAC902 chips, of which features are as follows:

- High Speed 165M Samples-per-second DAC
- One Single Ended Analog Output
- Single 5V or 3V Operation
- High SFDR(Spurious Free Dynamic Range) : 5MHz at 100MSPS
- Glueless DSP Interface

- Parallel Micro processor/DSP Interface
- Analog Output Range : $\pm 1V$

2.3. Address Decoding

Three addresses are assigned to AD/DA registers: ADC, DAC0 and DAC1, which are shown in Table 2. These address information is included in the header file addaio.h.

Table 2. AD/DA Address Mapping

DSP	Register	Chip Select	A3	A2	Write Enable	R/W	Address
C6711	ADC	0	0	X	X	R/W	CE2BASE+ 0x00000000
	DAC 0	0	1	0	0	W	CE2BASE+ 0x00000008
	DAC 1	0	1	1	0	W	CE2BASE+ 0x0000000C
C6701	ADC	0	0	X	X	R/W	CE1BASE + 0x00200000
	DAC 0	0	1	0	0	W	CE1BASE + 0x00200008
	DAC 1	0	1	1	0	W	CE1BASE + 0x0020000C
C6203	ADC	0	0	X	X	R/W	CE1BASE + 0x00200000
	DAC 0	0	1	0	0	W	CE1BASE + 0x00200008
	DAC 1	0	1	1	0	W	CE1BASE + 0x0020000C
C6416	ADC	0	0	X	X	R/W	ACE2BASE+ 0x00000000
	DAC 0	0	1	0	0	W	ACE2BASE+ 0x00000008
	DAC 1	0	1	1	0	W	ACE2BASE+ 0x0000000C

2.4. Pin Connector

The DSP STAR AD/DA connector is a 50 pin, 2 mm pitch connector. Table 3 and 0 present the connector pinouts, which complies to Texas Instrument Compliant Interface.

Table 3. AD/DA Connector Pinout

Connector 1 (CON1)				Connector 2 (CON2)			
Pin No.	Pin Name	Pin Name	Pin No.	Pin No.	Pin Name	Pin Name	Pin No.
1	NC	NC	2	1	5V	5V	2
3	GND	GND	4	3			4
5	5V	5V	6	5			6
7	GND	GND	8	7			8
9	5V	5V	10	9			10
11	NC	NC	12	11	GND	GND	12
13	NC	NC	14	13			14
15	NC	NC	16	15			16
17	NC	NC	18	17			18
19	3.3V	3.3V	20	19			20
21		NC	22	21	5V	5V	22
23			24	23			24
25	GND	GND	26	25	EA3	EA2	26
27		NC	28	27			28
29			30	29			30
31	GND	GND	32	31	GND	GND	32
33		NC	34	33			34
35			36	35			36
37	GND	GND	38	37			38
39		NC	40	39			40
41			42	41	3.3V	3.3V	42
43	GND	GND	44	43			44
45	TOUT0		46	45			46
47	NC		48	47			48
49	TOUT1		50	49			50
51	GND	GND	52	51	GND	GND	52
53		NC	54	53			54
55	NC	NC	56	55			56
57	NC	NC	58	57	ED11	ED10	58
59		NC	60	59	ED9	ED8	60
61	GND	GND	62	61	GND	GND	62
63			64	63	ED7	ED6	64
65			66	65	ED5	ED4	66
67		EXT_INT7	68	67	ED3	ED2	68
69	NC	NC	70	69	ED1	ED0	70
71	NC	NC	72	71	GND	GND	72
73	NC	NC	74	73	/ARE	/AWE	74
75	GND	GND	76	75			76
77	GND		78	77		/CE2	78
79	GND	GND	80	79	GND	GND	80

Table 4. Pin Descriptions of CON1, CON2

Pin Name	I/O	Description
BD[11..0]	I/O	External Data Bus
BA[3..2]	O	External Address Bus(used for address decoding)
/CE2	O	CE2 Memory Space Enable (used for address decoding)
/ARE	O	Memory Read Enable (ADC Read)
/AWE	O	Memory Write Enable (ADC/DAC Write)
EXT_INT7	I	External Interrupt 7 (connected to ADC Data Available Signal)
TOUT[1..0]	O	Timer Output(used as ADC/DAC Conversion Clock)
3.3V		3.3 V
5V		5V
GND		Ground

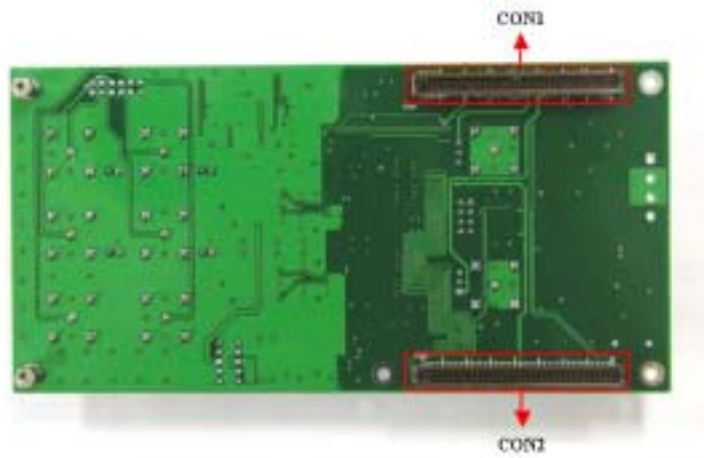


Figure 4. Physical Locations of CON1, CON2

2.5. Power Source

Power can be supplied externally or internally. External power of $\pm 12V$ can be supplied to the AD/DA module through the external power connector in Figure 3, in which case the power select switch should be made to the EXT side. When the power select switch is switched to the INT side, internal power is used for the AD/DA module. Table 5 and Table 6 show pinouts of the External Power Connector and Power Select Switch, respectively.

Table 5. External Power Connector Pinout

Pin No.	Description
1	External +12V
2	Ground
3	Ground
4	External -12V



Figure 5. Physical Location of External Power Connector

Table 6. Power Select Switch Pinout

Pin No.	Description	Description	Pin No.
1	INT_A5V	INT_N5V	4
3	A5V	-5V	6
2	EXT_A5V	EXT_N5V	5

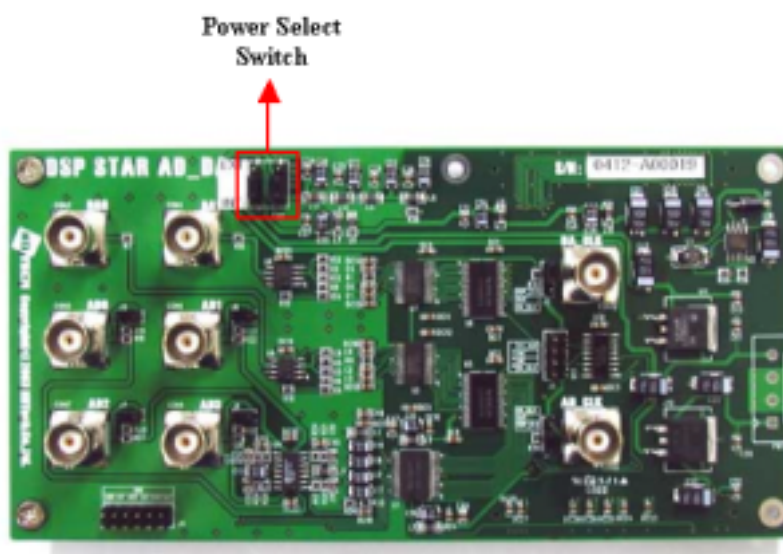


Figure 6. Physical Location of Power Select Switch

2.6. Clock Source

Clock is also supplied internally or externally to ADC or DAC. External clock can be separately supplied to DAC and ADC. For each of ADC and DAC, two types of clock connectors are present: BNC type connector and PIN type connector. When BNC connector is used for ADC or DAC, the corresponding jumper connector should be located at pin 2 and pin 3. When jumper connector is set at pin 1 and pin 2, DSP timer 0 (timer 1) clock is used as the clock source for the ADC (DAC) chip of the AD/DA module. The following two tables present pinouts of the AD_CLK Select Connector and the DA_CLK Select Connector.

Table 7. AD_CLK Select Connector

Pin No.	Description
1	TOUT0
2	AD_CLK
3	CON10

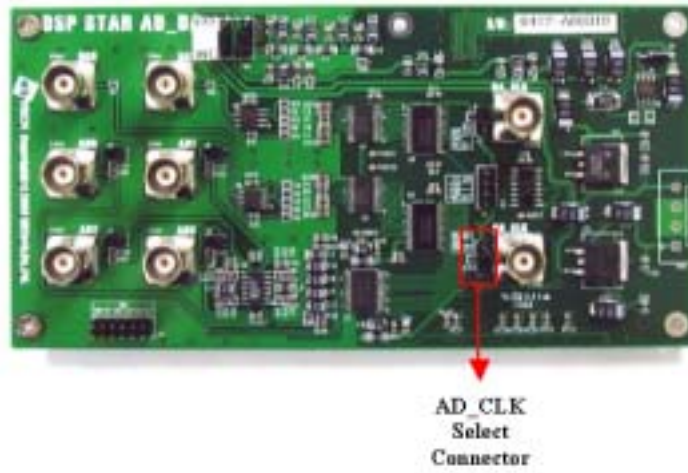


Figure 7. Physical Location of AD_CLK Select Connector

Table 8. DA_CLK Select Connector

Pin No.	Description
1	TOUT1
2	DA_CLK
3	CON9

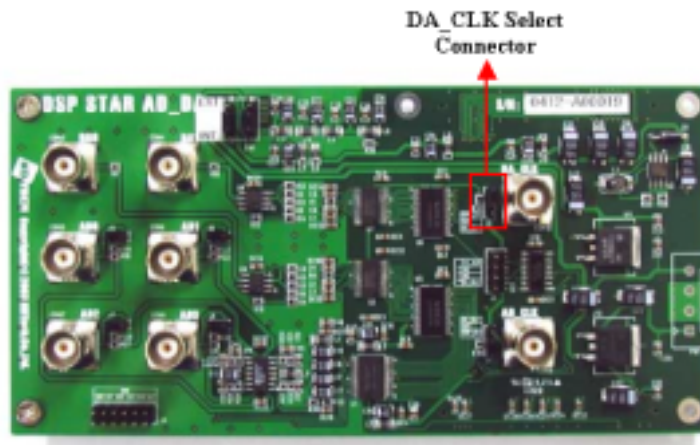


Figure 8. Physical Location of DA_CLK Select Connector

Table 9 shows pinout of the pin type connector.

Table 9. External Clock Pin Type Connector

Pin No.	Pin Name	Pin Name	Pin No.
1	EXT_AD_CLK	GND	2
3	NC	GND	4
5	NC	GND	6
7	EXT_DA_CLK	GND	8

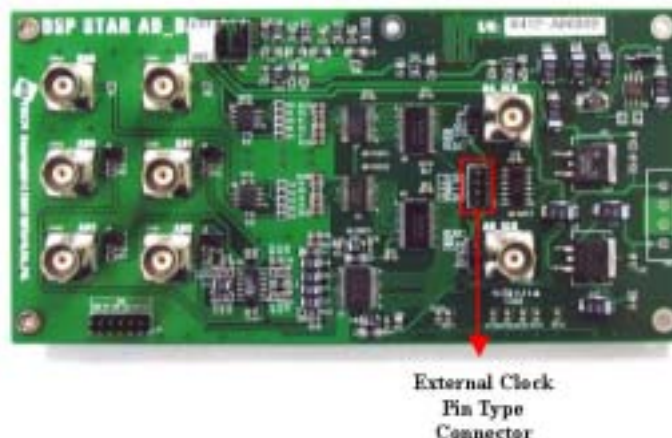


Figure 9. Physical Location of External Clock Pin Type Connector

2.7. Data In/Out

The DSP STAR AD/DA module contains BNC type of six analog connectors and pin type of six analog connectors for the analog data input and output operations. Table 10 lists pinout of six analog input/output BNC connectors, while Table 11 shows pinout of twelve-pin connector.

Table 10. AD/DA BNC Connector

Pin No.	Description
CON3	DAC Output 0
CON4	DAC Output 1
CON5	ADC Input 0
CON6	ADC Input 1
CON7	ADC Input 2
CON8	ADC Input 3

Table 11. AD/DA Pin Connector

Pin No.	Pin Name	Pin Name	Pin No.
1	AD0 Input	GND	2
3	AD1 Input	GND	4
5	AD2 Input	GND	6
7	AD3 Input	GND	8
9	DA0 Output	GND	10
11	DA1 Output	GND	12



Figure 11. Physical Location of AD/DA Pin Connector

2.8. 50 Ohm Termination On/Off

Table 12 presents pinout of 50 Ohm Termination On/Off Jumper. When the jumper is made ON, the 50 ohm termination is applied to the input signals.

Table 12. Termination Section Jumper

Jumper	Pin No.		ON/OFF	Description
J5	1	2	On	AD Input 0 : 50 ohm Termination made
			Off	AD Input 0 : No Termination made
J6	1	2	On	AD Input 1 : 50 ohm Termination made
			Off	AD Input 1 : No Termination made
J7	1	2	On	AD Input 2 : 50 ohm Termination made
			Off	AD Input 2 : No Termination made
J8	1	2	On	AD Input 3 : 50 ohm Termination made
			Off	AD Input 3 : No Termination made



Figure 12. Physical Location of Termination Section Jumper

2.9. Analog Input Schematic

In the Figure 13 below, R is 10 Kohm and all 4 channels are identical. Therefore input impedance becomes 10 Kohm

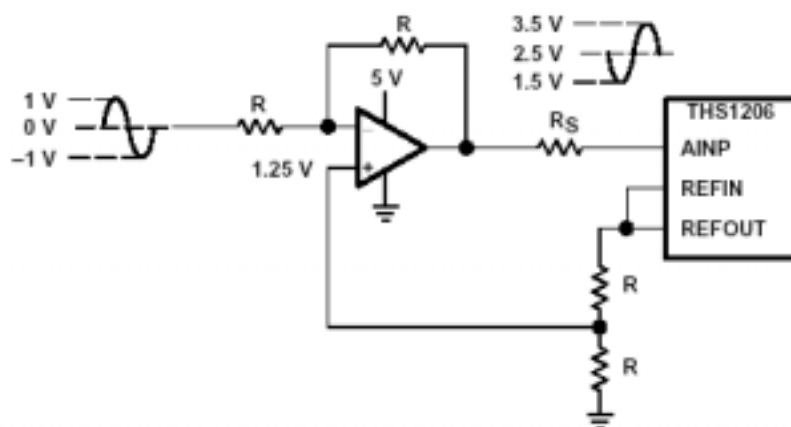


Figure 13. Analog Input Schematic

2.10. Analog Output Schematic

A 50 ohm register is added between Vout and Connector pin. Therefore output impedance is close to 50 ohm.

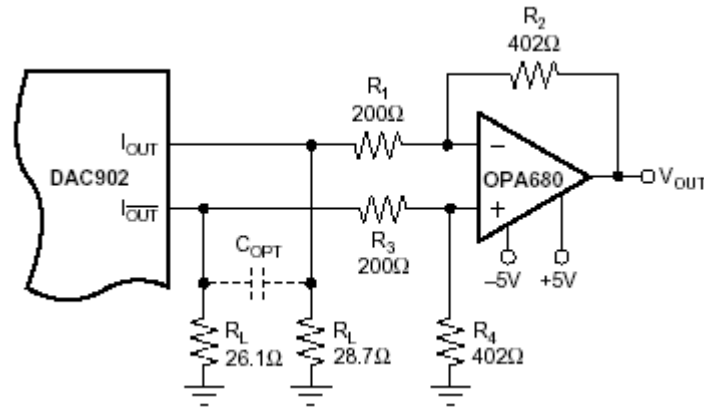


Figure 14. Analog Output Schematic

3. Control Registers

3.1. ADC Control Register

The THS 1206 contains two 10-bit wide control registers (CR0, CR1) in order to program the device into the desired mode. The bit definitions of both control registers are shown in Table 13.

Table 13. Bit Definitions of Control Register CR0 and CR1

REG	BIT9	BIT8	BIT7	BIT6	BIT5
CR0	TEST1	TEST0	SCAN	DIFF1	DIFF0
CR1	RBACK	OFFSET	BIN/2S	R/W	DATA_P
	BIT4	BIT3	BIT2	BIT1	BIT0
CR0	CHSEL1	CHSEL0	PD	MODE	VREF
CR1	DATA_T	TRIG1	TRIG0	OVFL/FRS T	RESET

Writing to control register 0 and control register 1

The 10-bit wide control register 0 and control register 1 can be programmed by addressing the desired control register and writing the register value to the ADC. The addressing is performed with the upper data bits D10 and D11, which function in the case as address line RA0 and RA1. During this write process, the data bits D0 through D9 contain the desired control register value.

Table 14. Control Register Addressing

D0-D9	D10/RA0	D11/RA1	Address
Desired register value	0	0	Control register 0
Desired register value	1	0	Control register 1
Desired register value	0	1	Reserved for future
Desired register value	1	1	Reserved for future

Table 15. Control Register 0

BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6
0	0	Test1	Test0	SCAN	DIFF1
BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIFF0	CHSEL1	CHSEL0	PD	MODE	VREF

Table 16. Control Register 0 Bit Functions

BITS	RESET	VALUE NAME	FUNCTION
0	0	VREF	Vref select: Bit 0 = 0 -> The internal reference is selected Bit 0 = 1 -> The external reference voltage is selected
1	0	MODE	Continuous conversion mode/single conversion mode Bit 1 = 0 -> Continuous conversion mode is selected. An external clock signal is applied to the CONV_CLK input in this mode. With every falling edge of the CONV_CLK signal a new converted value is written into the FIFO. Bit 1 = 1 -> Single conversion mode is selected In this mode, the CONV_CLK input functions as a CONVST input. A single conversion is initiated on the THS1206 by pulsing the CONVST input. On the falling edge of CONVST, the sample and hold stages of the selected analog inputs are placed into hold simultaneously, and the conversion sequence for the selected channels is started. The signal DATA_AV (data available) becomes active when the trigger condition is satisfied.
2	0	PD	Power down. Bit 2 = 0 -> The ADC is active Bit 2 = 1 -> Power down The reading and writing to and from the digital outputs is possible during power down. It is also possible to read out the FIFO.
3, 4	0,0	CHSEL0 CHSEL1	Channel select Bit 3 and bit 4 select the analog input channel of the ADC. Refer to Table 19.
5,6	1,0	DIFF0, DIFF1	Number of differential channels Bit 5 and bit 6 contain information about the number of selected differential channels. Refer to Table 19.
7	1,0	SCAN	Autoscan enable Bit 7 enables or disables the autoscan function of the ADC. Refer to Table 19.
8,9	0	TEST0, TEST1	Test input enable Bit 8 and bit 9 control the test function of the ADC. Three different test voltages can be measured. This feedback allows the check of all hardware connections and the ADC operation. To get the THS1206 back to the normal operating mode, apply the initialization routine.

Table 17. Control Register 1

BIT11	BIT10	BIT 9	BIT 8	BIT 7	BIT 6
0	1	RBACK	OFFSET	BIN/2s	R/W
BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
DATA_P	DATA_T	TRIG1	TRIG0	OVFL/FRST	RESET

Table 18. Control Register 1 Bit Functions

BITS	RESET VALUE	NAME	FUNCTION
0	0	RESET	Reset Writing a 1 into this bit resets the device and sets the control register 0 and control register 1 to the reset values. In addition the FIFO pointer and offset register is reset. After reset, it takes 5 clock cycles until the first value is converted and written into the FIFO.
1	0	OVFL (read only) FRST (write only)	Overflow flag (read only) Bit 1 of control register 1 indicates an overflow in the FIFO. Bit 1 = 0 -> no overflow occurred. Bit 1 = 1 -> an overflow occurred. This bit is reset to 0, after this control register is read from the processor. FRST: FIFO reset (write only) By writing a 1 into this bit, the FIFO is reset.
2,3	0, 0	TRIG0, TRIG1	FIFO trigger level Bit 2 and bit 3 of control register 1 are used to set the trigger level for the FIFO. If the trigger level is reached, the signal DATA_AV (data available) becomes active according to the settings of DATA_T and DATA_P. This indicates to the processor that the ADC values can be read. Refer to Table 20.
4	1	DATA_T	DATA_AV type Bit 4 of control register 1 controls whether the DATA_AV signal is a pulse or static (e.g for edge or level sensitive interrupt inputs). If it is set to 0, the DATA_AV signal is static. If it is set to 1, the DATA_AV signal is a pulse.
5	1	DATA_P	DATA_AV polarity Bit 5 of control register 1 controls the polarity of DATA_AV. If it is set to 1, DATA_AV is active high. If it is set to 0, DATA_AV is active low.
6	0	R/W	R/W, RD/WR selection Bit 6 of control register 1 controls the function of the inputs RD and WR. When bit 6 in control register 1 is set to 1, WR becomes a R/W input and RD is disabled. From now on a read is signalled with R/W high and a write with R/W as a low signal. If bit 6 in control register 1 is set to 0, the input RD becomes a read input and the input WR becomes a write input.
7	0	BIN/2s	Complement select If bit 7 of control register 1 is set to 0, the output value of the ADC is in twos complement. If bit 7 of control register 1 is set to 1, the output value of the ADC is in binary format.
8	0	OFFSET	Offset cancellation mode Bit 8 = 0 -> normal conversion mode Bit 8 = 1 -> offset calibration mode If a 1 is written into bit 8 of control register 1, the device internally sets the inputs to zero and does a conversion. The conversion result is stored in an offset register and subtracted from all conversions in order to reduce the offset error.
9	0	RBACK	Debug mode Bit 9 = 0 -> normal conversion mode Bit 9 = 1 -> enable debug mode When bit 9 of control register 1 is set to 1, debug mode is enabled. In this mode, the contents of control register 0 and control register 1 can be read back. The first read after bit 9 is set to 1 contains the value of control register 0. The second read after bit 9 is set to 1 contains the value of control register 1. To get the THS1206 back to the normal operating mode, apply the initialization routine.

3.2. Analog Input Channel Selection

The analog input channels of the THS1206 can be selected via bits 3 to 7 of control register 0. One single channel (single-ended or differential) is selected via bit 3 and bit 4 of control register 0. Bit 5 controls the selection between single-ended and differential configuration. Bit 6 and bit 7 select the autoscan mode, if more than one input channel is selected. Table 19 shows the possible selections.

Table 19. Analog Input Channel Configurations

BIT 7 SCAN	BIT 6 DIFF 1	BIT 5 DIFF 0	BIT 4 CHSEL 1	BIT 3 CHSEL 0	DESCRIPTION OF THE SELECTED INPUTS
0	0	0	0	0	Analog input AINP (single ended)
0	0	0	0	1	Analog input AINM (single ended)
0	0	0	1	0	Analog input BINP (single ended)
0	0	0	1	1	Analog input BINM (single ended)
0	0	1	0	0	Differential channel (AINP–AINM)
0	0	1	0	1	Differential channel (BINP–BINM)
1	0	0	0	1	Autoscan two single ended channels: AINP, AINM, AINP, ...
1	0	0	1	0	Autoscan three single ended channels: AINP, AINM, BINP, AINP, ...
1	0	0	1	1	Autoscan four single ended channels: AINP, AINM, BINP, BINM, AINP, ...
1	0	1	0	1	Autoscan one differential channel and one single ended channel AINP, (BINP–BINM), AINP, (BINP–BINM), ...
1	0	1	1	0	Autoscan one differential channel and two single ended channel AINP, AINM, (BINP–BINM), AINP, ...
1	1	0	0	1	Autoscan two differential channels (AINP–AINM), (BINP–BINM), (AINP–AINM), ...
0	0	1	1	0	Reserved
0	0	1	1	1	Reserved
1	0	0	0	0	Reserved
1	0	1	0	0	Reserved
1	0	1	1	1	Reserved
1	1	0	0	0	Reserved
1	1	0	1	0	Reserved
1	1	0	1	1	Reserved
1	1	1	0	0	Reserved
1	1	1	0	1	Reserved
1	1	1	1	0	Reserved
1	1	1	1	1	Reserved

3.3. FIFO Trigger Level

Bit 2 and bit 3 (TRIG1, TRIG0) of control register 1 are used to set the trigger level of the FIFO (see Table 20). If the trigger level is reached, the DATA_AV (data available) signal becomes active according to the setting of the signal DATA_AV to indicate to the processor that the ADC values can be read.

Table 20 shows four different programmable trigger levels for each configuration. The FIFO trigger level, which can be selected, is dependent on the number of input channels. Both, a differential or a single-ended input is considered as one channel. The processor therefore always reads the data from the FIFO in the same order and is able to distinguish between the channels.

Table 20. FIFO Trigger Level

BIT 3 TRIG 1	BIT 2 TRIG 0	TRIGGER LEVEL FOR 1 CHANNEL (ADC values)	TRIGGER LEVEL FOR 2 CHANNEL (ADC values)	TRIGGER LEVEL FOR 3 CHANNEL (ADC values)	TRIGGER LEVEL FOR 4 CHANNEL (ADC values)
0	0	01	02	02	04
0	1	04	04	06	08
1	0	08	08	09	12
1	1	14	12	12	Reserved

3.4. INITIALIZATION OF THE THS1206

The initialization of the THS1206 should be done according to the configuration flow shown in Figure 15.

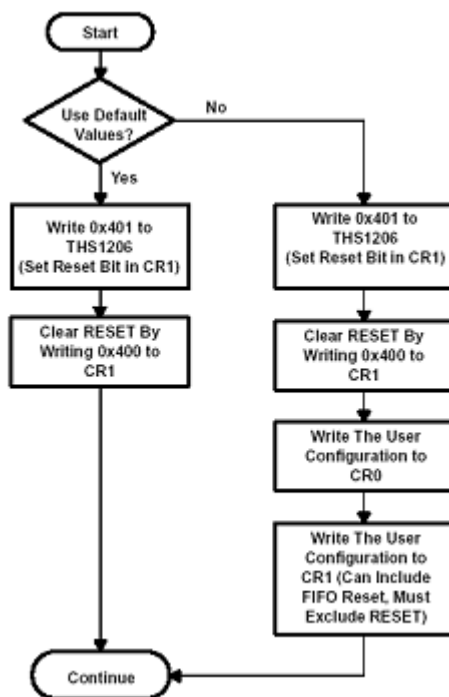


Figure 15. THS1206 Configuration Flow

3.5. DA Converter output voltage

The DAC902 provides two complementary current outputs, I_{out} , $-I_{out}$. These current outputs are applied to the circuit in Figure 14, and then converted to the output voltage V_{out} . Table 21 shows the relationship of input digital values and analog output signals.

Table 21. Input Code vs Analog Outputs

Input Code	I_{out}	$-I_{out}$	V_{out}
0xFFF	20mA	0mA	+1V
0x0C00			+0.5V
0x0800	10mA	10mA	0V
0x0400			-0.5V
0x0000	0mA	20mA	-1.0V

4. AD/DA Drive Software

In this section are explained interrupt mechanisms for AD/DA conversion as well as clock generation.

4.1. Analog-to-Digital Conversion

In order to employ AD part, it is necessary to write programs for each of three functions: AD clock generation, AD initialization, and Interrupt.

1. AD clock generation

Clock for AD can be supplied internally or externally, as described in section 2.6. When internal clock generation is selected in the hardware, timer clock 0 output is employed for A/D conversion. So, the program needs to include initialization routine of timer clock 0.

2. AD initialization

The program in the AD initialization sets up the number of AD channels through which input analog signals are entered into the board.

3. Interrupt

The DATA_AV signal of THS1206, which generates a pulse every scan cycle of AD conversions, is connected to external interrupt pin. The different pins are assigned depending on DSP Type, which is listed in Table 22. Therefore, it is very important that the number of AD reads in the interrupt service routine should match to the number of active channels pre-configured in the AD initialization routine.

Table 22. External Interrupt Pin Assignment

DSP Type	External Interrupt Assigned for Analog to Digital Conversion
C6711	EXT_INT7
C6701	EXT_INT4
C6203	EXT_INT4
C6416	EXT_INT7

4.2. Digital-to-Analog Conversion

DA channels operate independently, but work in synchronization. DA clock can also be provided internally, from timer clock 1. In such a case, initialization for timer clock 1 is needed. Timer clock 1 interrupt can then be used for writing to DA channels.

5. Example DSP Programs

The example programs are available in the product CD for six different hardware platforms listed in Figure 16. The folder “common” includes the header files used for all the example programs.

Figure 16. Example Program Folder

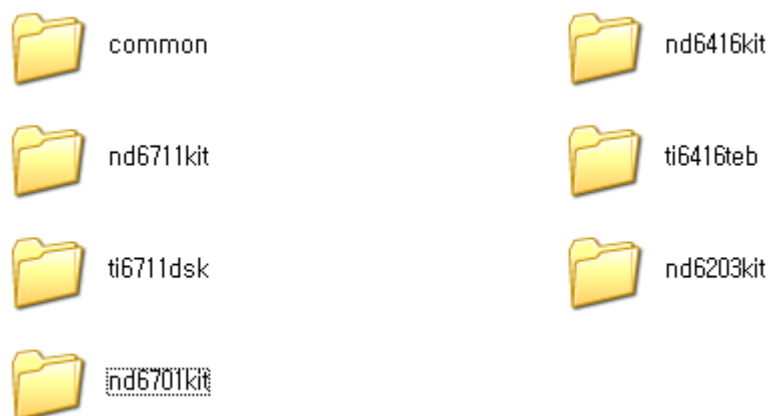


Table 23. Example DSP Programs

Folder Name	Descriptions
ad_dma_intr	Read 1 AD channel via EDMA and double buffer is used so that CPU can process the data, while DMA moves AD channel data to memory (only available for C6711 and C6416)
ad_dma_2ch	Read 2 AD channels and copy to DSP memory via DMA
ad_dma_4ch	Read 4 AD channels and copy to DSP memory via DMA
ad_intr_2ch	Read 2 AD channels and copy to DSP memory via interrupt
ad_intr_4ch	Read 4 AD channels and copy to DSP memory via interrupt
adda_dma_2ch	Loop 2 AD channels into 2 DA channels via DMA
adda_intr_2ch	Loop 2 AD channels into 2 DA channels via interrupt
adda_intr_4ch	Loop 4 AD channels into 4 DA channels via interrupt
da_intr_saw	Send saw waveform to DA via interrupt
da_intr_sine	Send sine waveform to DA via interrupt