

# DSP STAR Kit User's Manual

Revision 2.9

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## 1. DSP STA Kit System

DSP STAR Kit (DSK) is a development board using Texas Instrument's C6000 DSP processor. Several kit models are now available to meet various requirements of the target applications. Except DSP processor, other board devices are the same for all of the models such as external SDRAM of size 16Mbyte (DS6203K, DS6701K) or 32Mbyte (DS6416K), 1Mbyte Flash ROM, a stereo codec providing 16/24/32-bit 8~96KHz sampling for high quality voice or audio processing, user RS232 port, JTAG port and expansion port compatible to TI Daughter Card Interface.

DSK is not just a hardware board but a complete development system containing its own free bundle debugger named Code Builder IDE. User's application program can be developed using either RS232-based Code Builder or J-TAG based Code Composer Studio.

Code Builder IDE connects the PC to DSK hardware board via RS232 serial interface, which provides the programmer program editing, executable code generation using TI C6000 codegen utilities, program download, debugging, flash read/write/erase, data plot, disassembly view, breakpoint setting, memory edit/view/fill, register view, image view, data load from file to memory, memory data write to file and so on through convenient Graphic User Interface. More information is included in the Code Builder user's manual.

## 2. DSP STAR Kit Hardware

### 2.1. Hardware Board Description

DSP STAR Kit hardware is provided as one board, as shown in Figure 1, in which are contained memory, audio codec, two serial ports, LEDs, DIP switches, and the interface connector. The interface connectors comply to Texas Instrument's Daughter Card Interface. Key features of the hardware are shown in Table 1.

Table 1. Key Features

DSP	C6711 <sup>1</sup> , C6701, C6203, C6416
Serial Ports	Two RS232 Serial Ports (User Port, Code Builder Port)
Codec	TLV320AIC23(16/24/32 bit Stereo Audio Codec, 8~96KHz with integrated Headphone Amplifier)
LED	1 Power LED, 1 Reset LED, 4 User LED
Switch	One 4-Pin DIP Switch
Interface Connector	Texas Instrument Expansion Daughter Card Interface

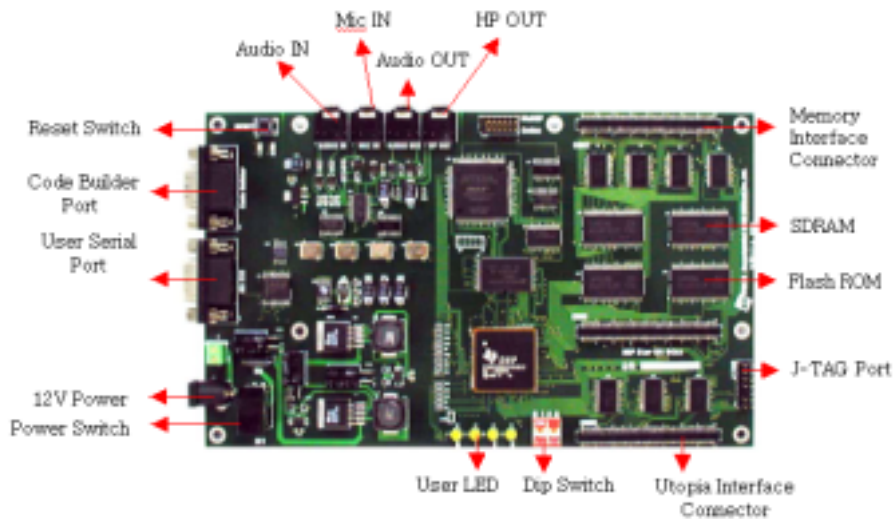


Figure 1. Real Image of DSP STAR Kit Board

<sup>1</sup> Obsolete since August, 2005

## 2.2. Hardware Components

### 2.2.1. Audio Codec

The TLV320AIC23 audio codec chip is used in the DSPS TAR Kit board and its features are as follows:

- 8KHz ~ 96KHz Sample Frequency Support
- 16/20/24/32-bits Word Length
- Glueless Interface to TI McBSPs
- Stereo Line Input/Output
- ADC Multiplexed Input for Stereo-Line Input and Microphone
- Analog Volume Control with Mute
- Highly Efficient Linear Headphone Amplifier

The following Table 2 lists the control registers for audio.

Table 2. Audio Codec Control Register

Address	Register
0000000	Left Line Input Channel Volume Control Register
0000001	Right Line Input Channel Volume Control Register
0000010	Left Channel Headphone Volume Control Register
0000011	Right Channel Headphone Volume Control Register
0000100	Analog Audio Path Control Register
0000101	Digital Audio Path Control Register
0000110	Power Down Control Register
0000111	Digital Audio Interface format Register
0001000	Sample Rate Control Register
0001001	Digital Interface Activation Register
0001111	Reset Register

Data path from/to audio codec is directly connected to McBSP ports. Data format can be decided by the value of the Digital Audio Interface format Register in Table 2. Writing values to the control registers is done indirectly via the 3-bit register as shown in Table 3. This register is called Codec Serial Data Write Register, implemented with EPLD in kit hardware.

Table 3. Codec Serial Data Write Register

Name	R/W	Data	Description
Codec	R/W	D[2..0]	D[2] : Codec Chip Select 0 : Chip Select Low 1 : Chip Select High D[1] : Codec Serial Clock 0 : Chip Serial Clock Low 1 : Chip Serial Clock High D[0] : Codec Serial Data 0 : Chip Serial Data Low 1 : Chip Serial Data High

### 2.2.2. Serial Port

There are two serial connections between the host computer and the hardware board. One connection is via the Asynchronous Serial Port, connected to the data bus of DSP processor. This connection allows the user debug and monitor the processor. The other serial connection is used for Code Builder.

Two registers of 6-bit RS232C control register and 8-bit RS232D data register realize asynchronous serial port. The bit definitions of these two registers are described in Table 4. When data arrives at the user serial port, external interrupt 7 is generated.

Table 4. Asynchronous Serial Port Control/Data Registers

Name	R/W	Data	Description
RS232C	W	D[3..0]	D[3] : Tx Interrupt D[2] : Rx Interrupt D[1..0] : Baud Rate 00 : 9600Bps 01 : 19200Bps 10 : 57600Bps 11 : 115200Bps
	R	D[5..0]	D[5] : Tx Ready D[4] : Rx Ready D[3] : Tx Interrupt D[2] : Rx Interrupt D[1..0] : Baud Rate 00 : 9600Bps 01 : 19200Bps 10 : 57600Bps 11 : 115200Bps
RS232D	W	D[7..0]	D[7..0] : Tx Data
	R	D[7..0]	D[7..0] : Rx Data

### 2.2.3. On board Memory

The kit hardware includes two types of memory, SDRAM and Flash memory. 0 lists memory sizes for various kit model.

Table 5. Memory Size

Model	Memory
DSK6701	16M Bytes SDRAM, 1M Bytes Flash Memory
DSK6203	16M Bytes SDRAM, 1M Bytes Flash Memory
DSK6416	32M Bytes SDRAM, 1M Bytes Flash Memory

### 2.2.4. User LED

Each of four LED's is turned on/off according to four bit values of LED register. When the bit is 1 (0), the LED is turned on (off). Each bit of LED register is explained in Table 6.

Table 6. LED Register

Name	R/W	Data	Description
LED	R/W	D[3..0]	D[3] : LED[3] D[2] : LED[2] D[1] : LED[1] D[0] : LED[0]

### 2.2.5. User Switch

The kit board contains four DIP switches, which can be set through the Switch Input Register in Table 7. When the switch is ON (OFF), the register value is read as '1' ('0'). This register is Read Only.

Table 7. Switch Input Register

Name	R/W	Data	Description
SW	R	D[3..0]	D[3] : SW[3] D[2] : SW[2] D[1] : SW[1] D[0] : SW[0]

### 2.2.6. Interface Connector

The kit board contains memory interface connector and peripheral interface connector as shown in Figure 1. Additionally, DSK6416 includes UTOPIA connection. Pin descriptions are contained in the tables of section 3.2.

### 2.2.7. Reset and Power Switches

The kit hardware takes 12V (500mA) external power source. Switching regulator is used to supply needed power for the devices in the hardware board. In the board is included the power switch displaying power on/off status. Also, the board reset switch is included to reset DSP and board devices.

### 3. Appendix A

#### 3.1. Kit Specifications

Table 8. Technical Specifications

	<b>DSK 6701</b>	<b>DSK 6203</b>	<b>DSK 6416</b>
<b>Math</b>	Floating Point	Fixed Point	Fixed Point
<b>Processing Speed</b>	900 MFLOPS	2400 MIPS	4800 MIPS
<b>Internal Memory</b>	128K byte	896K byte	1M byte
<b>External Memory</b>	16Mbyte SDRAM 1Mbyte Flash ROM		32Mbyte SDRAM 1Mbyte Flash ROM
<b>Codec</b>	TLV320AIC23, 16/24/32 bit stereo audio codec, 8 ~ 96k samples/second		
<b>Serial Port</b>	2 Multi channel Buffered Serial Port 1 Asynchronous Serial Port		
<b>Timer</b>	2 32-bit Timer		3 32-bit Timer
<b>J-TAG</b>	J-TAG Port		
<b>Debugger</b>	Code Builder IDE		

### 3.2. Interface Connector and Pin Description

Table 9. DSK6701 Interface Connector

Connector 1(Peripheral)				Connector 2(Memory)			
Pin No.	Pin Name	Pin Name	Pin No.	Pin No.	Pin Name	Pin Name	Pin No.
1	NC	NC	2	1	5V	5V	2
3	GND	GND	4	3	EA21	EA20	4
5	5V	5V	6	5	EA19	EA18	6
7	GND	GND	8	7	EA17	EA16	8
9	5V	5V	10	9	EA15	EA14	10
11	NC	NC	12	11	GND	GND	12
13	NC	NC	14	13	EA13	EA12	14
15	NC	NC	16	15	EA11	EA10	16
17	NC	NC	18	17	EA9	EA8	18
19	3.3V	3.3V	20	19	EA7	EA6	20
21	CLKX0	NC	22	21	5V	5V	22
23	FSX0	DX0	24	23	EA5	EA4	24
25	GND	GND	26	25	EA3	EA2	26
27	CLKR0	NC	28	27	/BE3	/BE2	28
29	FSR0	DR0	30	29	/BE1	/BE0	30
31	GND	GND	32	31	GND	GND	32
33	CLKX1	NC	34	33	ED31	ED30	34
35	FSX1	DX1	36	35	ED29	ED28	36
37	GND	GND	38	37	ED27	ED26	38
39	CLK1	NC	40	39	ED25	ED24	40
41	FSR1	DR1	42	41	3.3V	3.3V	42
43	GND	GND	44	43	ED23	ED22	44
45	TOUT0	TINP0	46	45	ED21	ED20	46
47	NC	EXT_INT6	48	47	ED19	ED18	48
49	TOUT1	TINP1	50	49	ED17	ED16	50
51	GND	GND	52	51	GND	GND	52
53	EXT_INT7	LACK	54	53	ED15	ED14	54
55	INUM3	INUM2	56	55	ED13	ED12	56
57	INUM1	INUM0	58	57	ED11	ED10	58
59	/RESET	PD	60	59	ED9	ED8	60
61	GND	GND	62	61	GND	GND	62

63	CNTL1	CNTL0	64	63	ED7	ED6	64
65	STAT1	STAT0	66	65	ED5	ED4	66
67	EXT_INT5	EXT_INT4	68	67	ED3	ED2	68
69	/CE2	/CE3	70	69	ED1	ED0	70
71	DMAC3	DAMC2	72	71	GND	GND	72
73	DMAC1	DMAC0	74	73	/ARE	/AWE	74
75	GND	GND	76	75	/AOE	ARDY	76
77	GND	CLKOUT2	78	77	NC	/CE1	78
79	GND	GND	80	79	GND	GND	80

Table 10. DSK6701 Connector Pin Description

Pin Name	I/O	Description
BD[31..0]	I/O	External Data Bus
BA[21..2]	O	External Address Bus
/CE1	O	CE1 Memory Space Enable
/CE2	O	CE2 Memory Space Enable
/CE3	O	CE3 Memory Space Enable
/ARE	O	Memory Read Enable
/AOE	O	Memory Output Enable
/AWE	O	Memory Write Enable
ARDY	I	Ready
/BE[3..0]	O	Byte Enable
EXT_INT[7..4]	I	External Interrupt
CLKOUT2	O	CPU Clock Output
CLKX0	I/O	McBSP 0 Transmit Clock
FSX0	I/O	McBSP 0 Transmit Frame Sync.
DX0	O	McBSP 0 Transmit Data
CLKR0	I/O	McBSP 0 Receive Clock
FSR0	I/O	McBSP 0 Receive Frame Sync.
DR0	I	McBSP 0 Receive Data
CLKX1	I/O	McBSP 1 Transmit Clock
FSX1	I/O	McBSP 1 Transmit Frame Sync.
DX1	O	McBSP 1 Transmit Data
CLKR1	I/O	McBSP 1 Receive Clock
FSR1	I/O	McBSP 1 Receive Frame Sync.
DR1	I	McBSP 1 Receive Data
TINP[1..0]	I	Timer Input
TOUT[1..0]	O	Timer Output
PD	O	Power Down Mode 3
IACK	O	Interrupt Acknowledge
INUM[3..0]	O	Active Interrupt Identification Number
DMAC[3..0]	O	DMA Action Complete
/RESET	O	Reset
CNTL[1..0]	O	Control Output
STAT[1..0]	O	Status Output
3.3V		3.3 V
5V		5V
GND		Ground

Table 11. DSK6203 Interface Connector

Connector 1(Peripheral)				Connector 2(Memory)			
Pin No.	Pin Name	Pin Name	Pin No.	Pin No.	Pin Name	Pin Name	Pin No.
1	NC	NC	2	1	5V	5V	2
3	GND	GND	4	3	EA21	EA20	4
5	5V	5V	6	5	EA19	EA18	6
7	GND	GND	8	7	EA17	EA16	8
9	5V	5V	10	9	EA15	EA14	10
11	NC	NC	12	11	GND	GND	12
13	NC	NC	14	13	EA13	EA12	14
15	NC	NC	16	15	EA11	EA10	16
17	NC	NC	18	17	EA9	EA8	18
19	3.3V	3.3V	20	19	EA7	EA6	20
21	CLKX0	NC	22	21	5V	5V	22
23	FSX0	DX0	24	23	EA5	EA4	24
25	GND	GND	26	25	EA3	EA2	26
27	CLKR0	NC	28	27	/BE3	/BE2	28
29	FSR0	DR0	30	29	/BE1	/BE0	30
31	GND	GND	32	31	GND	GND	32
33	CLKX1	NC	34	33	ED31	ED30	34
35	FSX1	DX1	36	35	ED29	ED28	36
37	GND	GND	38	37	ED27	ED26	38
39	CLK1	NC	40	39	ED25	ED24	40
41	FSR1	DR1	42	41	3.3V	3.3V	42
43	GND	GND	44	43	ED23	ED22	44
45	TOUT0	TINP0	46	45	ED21	ED20	46
47	NC	EXT_INT6	48	47	ED19	ED18	48
49	TOUT1	TINP1	50	49	ED17	ED16	50
51	GND	GND	52	51	GND	GND	52
53	EXT_INT7	LACK	54	53	ED15	ED14	54
55	INUM3	INUM2	56	55	ED13	ED12	56
57	INUM1	INUM0	58	57	ED11	ED10	58
59	/RESET	PD	60	59	ED9	ED8	60
61	GND	GND	62	61	GND	GND	62
63	CNTL1	CNTL0	64	63	ED7	ED6	64
65	STAT1	STAT0	66	65	ED5	ED4	66
67	EXT_INT5	EXT_INT4	68	67	ED3	ED2	68

69	/CE2	/CE3	70	69	ED1	ED0	70
71	DMAC3	DAMC2	72	71	GND	GND	72
73	DMAC1	DMAC0	74	73	/ARE	/AWE	74
75	GND	GND	76	75	/AOE	ARDY	76
77	GND	CLKOUT2	78	77	NC	/CE1	78
79	GND	GND	80	79	GND	GND	80

Table 12. DSK6203 Connector Pin Description

Pin Name	I/O	Description
BD[31..0]	I/O	External Data Bus
BA[21..2]	O	External Address Bus
/CE1	O	CE1 Memory Space Enable
/CE2	O	CE2 Memory Space Enable
/CE3	O	CE3 Memory Space Enable
/ARE	O	Memory Read Enable
/AOE	O	Memory Output Enable
/AWE	O	Memory Write Enable
ARDY	I	Ready
/BE[3..0]	O	Byte Enable
EXT_INT[7..4]	I	External Interrupt
CLKOUT2	O	CPU Clock Output
CLKX0	I/O	McBSP 0 Transmit Clock
FSX0	I/O	McBSP 0 Transmit Frame Sync.
DX0	O	McBSP 0 Transmit Data
CLKR0	I/O	McBSP 0 Receive Clock
FSR0	I/O	McBSP 0 Receive Frame Sync.
DR0	I	McBSP 0 Receive Data
CLKX1	I/O	McBSP 1 Transmit Clock
FSX1	I/O	McBSP 1 Transmit Frame Sync.
DX1	O	McBSP 1 Transmit Data
CLKR1	I/O	McBSP 1 Receive Clock
FSR1	I/O	McBSP 1 Receive Frame Sync.
DR1	I	McBSP 1 Receive Data
TINP[1..0]	I	Timer Input
TOUT[1..0]	O	Timer Output
PD	O	Power Down Mode 3
IACK	O	Interrupt Acknowledge
INUM[3..0]	O	Active Interrupt Identification Number
DMAC[3..0]	O	DMA Action Complete
/RESET	O	Reset
CNTL[1..0]	O	Control Output
STAT[1..0]	O	Status Output
3.3V		3.3 V
5V		5V
GND		Ground

Table 13. DSK6416 Interface Connector

Connector 1(Peripheral)				Connector 2(Memory)			
Pin No.	Pin Name	Pin Name	Pin No.	Pin No.	Pin Name	Pin Name	Pin No.
1	NC	NC	2	1	5V	5V	2
3	GND	GND	4	3	EA22	EA20	4
5	5V	5V	6	5	EA20	EA18	6
7	GND	GND	8	7	EA18	EA16	8
9	5V	5V	10	9	EA16	EA14	10
11	NC	NC	12	11	GND	GND	12
13	NC	NC	14	13	EA14	EA12	14
15	NC	NC	16	15	EA12	EA10	16
17	NC	NC	18	17	EA10	EA8	18
19	3.3V	3.3V	20	19	EA8	EA6	20
21	CLKX0	CLKS0	22	21	5V	5V	22
23	FSX0	DX0	24	23	EA6	EA4	24
25	GND	GND	26	25	EA4	EA2	26
27	CLKR0	NC	28	27	/BE3	/BE2	28
29	FSR0	DR0	30	29	/BE1	/BE0	30
31	GND	GND	32	31	GND	GND	32
33	CLKX2	CLKS2	34	33	ED31	ED30	34
35	FSX2	DX2	36	35	ED29	ED28	36
37	GND	GND	38	37	ED27	ED26	38
39	CLKR2	NC	40	39	ED25	ED24	40
41	FSR2	DR2	42	41	3.3V	3.3V	42
43	GND	GND	44	43	ED23	ED22	44
45	TOUT0	TINP0	46	45	ED21	ED20	46
47	NC	EXT_INT5	48	47	ED19	ED18	48
49	TOUT1	TINP1	50	49	ED17	ED16	50
51	GND	GND	52	51	GND	GND	52
53	EXT_INT4	NC	54	53	ED15	ED14	54
55	NC	NC	56	55	ED13	ED12	56
57	NC	NC	58	57	ED11	ED10	58
59	/RESET	NC	60	59	ED9	ED8	60
61	GND	GND	62	61	GND	GND	62
63	CNTL1	CNTL0	64	63	ED7	ED6	64
65	STAT1	STAT0	66	65	ED5	ED4	66
67	EXT_INT6	EXT_INT7	68	67	ED3	ED2	68
69	/CE3	NC	70	69	ED1	ED0	70

71	NC	NC	72	71	GND	GND	72
73	NC	NC	74	73	/ARE	/AWE	74
75	DET	GND	76	75	/AOE	ARDY	76
77	GND	AECLKOUT2	78	77	/CE3	/CE2	78
79	GND	GND	80	79	GND	GND	80

**Connector 3 (UTOPIA)**

Pin No.	Pin Name	Pin Name	Pin No.
1	GND	UXADDR4	2
3	UXADDR3	UXADDR2	4
5	UXADDR1	UXADDR0	6
7	NC	NC	8
9	NC	NC	10
11	GND	NC	12
13	NC	NC	14
15	NC	NC	16
17	NC	NC	18
19	NC	NC	20
21	NC	NC	22
23	NC	NC	24
25	GND	UXSOC	26
27	UXDATA7	UXDATA6	28
29	UXDATA5	UXDATA4	30
31	UXDATA3	UXDATA2	32
33	UXDATA1	UXDATA0	34
35	UXCLAV	NC	36
37	GND	GND	38
39	UXCLK	NC	40
41	GND	URADDR4	42
43	URADDR3	URADDR2	44
45	URADDR1	URADDR0	46
47	NC	NC	48
49	NC	NC	50
51	GND	NC	52
53	NC	NC	54
55	NC	NC	56
57	NC	NC	58

59	NC	NC	60
61	NC	NC	62
63	NC	NC	64
65	GND	URSOC	66
67	URDATA7	URDATA6	68
69	URDATA5	URDATA4	70
71	URDATA3	URDATA2	72
73	URDATA1	URDATA0	74
75	URCLAV	NC	76
77	GND	/URENB	78
79	URCLK	NC	80

Table 14. DSK6416 Connector Pin Description

Pin Name	I/O	Description
BD[31..0]	I/O	External Data Bus
BA[22..3]	O	External Address Bus
/CE1	O	CE1 Memory Space Enable
/CE2	O	CE2 Memory Space Enable
/CE3	O	CE3 Memory Space Enable
/ARE	O	Memory Read Enable
/AOE	O	Memory Output Enable
/AWE	O	Memory Write Enable
ARDY	I	Ready
/BE[3..0]	O	Byte Enable
EXT_INT[7..4]	I	External Interrupt
CLKOUT2	O	CPU Clock Output
CLKX0	I/O	McBSP 0 Transmit Clock
FSX0	I/O	McBSP 0 Transmit Frame Sync.
DX0	O	McBSP 0 Transmit Data
CLKR0	I/O	McBSP 0 Receive Clock
FSR0	I/O	McBSP 0 Receive Frame Sync.
DR0	I	McBSP 0 Receive Data
CLKX1	I/O	McBSP 1 Transmit Clock
FSX1	I/O	McBSP 1 Transmit Frame Sync.
DX1	O	McBSP 1 Transmit Data
CLKR1	I/O	McBSP 1 Receive Clock
FSR1	I/O	McBSP 1 Receive Frame Sync.
DR1	I	McBSP 1 Receive Data
TINP[1..0]	I	Timer Input
TOUT[1..0]	O	Timer Output
/RESET	O	Reset
CNTL[1..0]	O	Control Output
STAT[1..0]	O	Status Output
UXADDR[4..0]	I	UTOPIA Transmit Address
UXDATA[7..0]	O	UTOPIA Transmit Data
UXSOC	O	Transmit Start-of-Cell Signal
UXCLAV	O	Transmit Cell Available Status Output Signal
/UXENB	I	UTOPIA Transmit Enable Input Signal
UXCLK	I	Source Clock for UTOPIA Transmit
URADDR[4..0]	I	UTOPIA Receive Address

URDATA[7..0]	I	UTOPIA Receive Data
URSOC	O	Receive Start-of-Cell Signal
URCLAV	O	Receive Cell Available Status Output Signal
/URENB	I	UTOPIA Receive Enable Input Signal
URCLK	I	Source Clock for UTOPIA Receive
3.3V		3.3 V
5V		5V
GND		Ground

### 3.3. Memory Map

Table 15. DSK6701 Memory Map

Address	Description
0x00000000 ~ 0x0000FFFF	Internal Program RAM ( 64K Bytes)
0x00010000 ~ 0x0003FFFF	Reserved (4M - 64K Bytes)
0x00040000 ~ 0x013FFFFFFF	SDRAM(16M Bytes)
0x01400000 ~ 0x015FFFFFFF	Flash Memory (2M Bytes)
0x01600000 ~ 0x017FFFE8	Reserved (1M Bytes)
0x017FFFE8	Switch Input Register(4 Bytes)
0x017FFFF0	LED, CNTL, STAT Register (4 Bytes)
0x017FFFF4	Codec Initialize Register (4 Bytes)
0x017FFFF8	RS232 Data Register (4 Bytes)
0x017FFFFC	RS232 Control Register (4 Bytes)
0x01800000 ~ 0x0183FFFF	EMIF Registers(256K Bytes)
0x01840000 ~ 0x0187FFFF	DMA Control Registers(256K Bytes)
0x01880000 ~ 0x018BFFFF	HPI Registers(256K Bytes)
0x018C0000 ~ 0x018FFFFFFF	McBSP 0 Registers(256K Bytes)
0x01900000 ~ 0x0193FFFF	McBSP 1 Registers(256K Bytes)
0x01940000 ~ 0x0197FFFF	TIMER 0 Registers(256K Bytes)
0x01980000 ~ 0x019BFFFF	TIMER 1 Registers(256K Bytes)
0x019C0000 ~ 0x019FFFFFFF	Interrupt Select Registers(256K Bytes)
0x01A00000 ~ 0x01FFFFFFF	Reserved(6M Bytes)
0x02000000 ~ 0x02FFFFFFF	CE2(16M Bytes)
0x03000000 ~ 0x03FFFFFFF	CE3(16M Bytes)
0x04000000 ~ 0x07FFFFFFF	Reserved(2G – 64M Bytes)
0x80000000 ~ 0x803FFFFFFF	Internal Data RAM(64K Bytes)
0x80400000 ~ 0xFFFFFFFF	Reserved(2G – 64M Bytes)

Table 16. DSK6203 Memory Map

Address	Description
0x00000000 ~ 0x0005FFFF	Internal Program RAM ( 384K Bytes)
0x00060000 ~ 0x003FFFFFFF	Reserved (4M - 384K Bytes)
0x00400000 ~ 0x013FFFFFFF	SDRAM(16M Bytes)
0x01400000 ~ 0x015FFFFFFF	Flash Memory (2M Bytes)
0x01600000 ~ 0x017FFFE8	Reserved (2M – 20Bytes)
0x017FFFE8	Switch Input Register (4 Bytes)
0x017FFFF0	LED, CNTL, STAT Register (4 Bytes)
0x017FFFF4	Codec Initialize Register (4 Bytes)
0x017FFFF8	RS232 Data Register (4 Bytes)
0x017FFFFC	RS232 Control Register (4 Bytes)
0x01800000 ~ 0x0183FFFF	EMIF Registers(256K Bytes)
0x01840000 ~ 0x0187FFFF	DMA Control Registers(256K Bytes)
0x01880000 ~ 0x018BFFFF	HPI Registers(256K Bytes)
0x018C0000 ~ 0x018FFFFF	McBSP 0 Registers(256K Bytes)
0x01900000 ~ 0x0193FFFF	McBSP 1 Registers(256K Bytes)
0x01940000 ~ 0x0197FFFF	TIMER 0 Registers(256K Bytes)
0x01980000 ~ 0x019BFFFF	TIMER 1 Registers(256K Bytes)
0x019C0000 ~ 0x019FFFFF	Interrupt Select Registers(256K Bytes)
0x01A00000 ~ 0x01FFFFFF	Reserved(6M Bytes)
0x02000000 ~ 0x02FFFFFF	CE2(16M Bytes)
0x03000000 ~ 0x03FFFFFF	CE3(16M Bytes)
0x04000000 ~ 0x3FFFFFFF	Reserved(1G – 64M Bytes)
0x40000000 ~ 0x4FFFFFFF	Expansion Bus XCE0(256M Bytes)
0x50000000 ~ 0x5FFFFFFF	Expansion Bus XCE1(256M Bytes)
0x60000000 ~ 0x6FFFFFFF	Expansion Bus XCE2(256M Bytes)
0x70000000 ~ 0x7FFFFFFF	Expansion Bus XCE3(256M Bytes)
0x80000000 ~ 0x807FFFFF	Internal Data RAM(512K Bytes)
0x80800000 ~ 0xFFFFFFFF	Reserved(2G – 128K Bytes)

Table 17. DSK6416 Memory Map

Address	Description
0x00000000 ~ 0x000FFFFFFF	Internal RAM (L2 1M Bytes)
0x00100000 ~ 0x017FFFFFFF	Reserved (23M Bytes)
0x01800000 ~ 0x0183FFFFFF	EMIFA Registers (256K Bytes)
0x01840000 ~ 0x0187FFFFFF	L2 Control Registers(256K Bytes)
0x01880000 ~ 0x018BFFFFFF	HPI Control Registers(256K Bytes)
0x018C0000 ~ 0x018FFFFFFF	McBSP Port 0 Control Registers(256K Bytes)
0x01900000 ~ 0x0193FFFFFF	McBSP Port 1 Control Registers(256K Bytes)
0x01940000 ~ 0x0197FFFFFF	TIMER 0 Control Registers(256K Bytes)
0x01980000 ~ 0x019BFFFFFF	TIMER 1 Control Registers(256K Bytes)
0x019CFFFFFF ~ 0x019FFFFFFF	Interrupt Select Registers(256K Bytes)
0x01A00000 ~ 0x01A3FFFFFF	EDMA RAM and Registers(256K Bytes)
0x01A40000 ~ 0x01A7FFFFFF	McBSP Port 1 Control Registers(256K Bytes)
0x01A80000 ~ 0x01ABFFFFFF	EMIFB Registers(256K Bytes)
0x01AC0000 ~ 0x01AFFFFFFF	TIMER 2 Control Register(256K Bytes)
0x01B00000 ~ 0x01B3FFFFFF	GPIO Register(256K Bytes)
0x01B40000 ~ 0x01B7FFFFFF	UTOPIA Register(256K Bytes)
0x01B80000 ~ 0x01BFFFFFFF	Reserved(512K Bytes)
0x01C00000 ~ 0x01C3FFFFFF	PCI Register(256K Bytes)
0x01C40000 ~ 0x01FFFFFFF	Reserved(4M - 256K Bytes)
0x02000000 ~ 0x02000033	QDMA Register(52 Bytes)
0x02000034 ~ 0x2FFFFFFF	Reserved(736M – 52 Bytes)
0x30000000 ~ 0x33FFFFFFF	McBSP 0 Data(64M Bytes)
0x34000000 ~ 0x37FFFFFFF	McBSP 1 Data(64M Bytes)
0x38000000 ~ 0x3BFFFFFFF	McBSP 2 Data(64M Bytes)
0x3C000000 ~ 0x3FFFFFFF	UTOPIA Queues(64M Bytes)
0x40000000 ~ 0x5FFFFFFF	Reserved(512M Bytes)
0x60000000 ~ 0x63FFFFFFF	EMIFB CE0 (1M Bytes)
0x64000000 ~ 0x64FFFFFFF	Flash Memory (1M Byte)
0x64100000 ~ 0x67FFFFFFF	Reserved
0x6800001C	Switch Input Register (4 Byte)
0x68000020	LED, CMTL, STAT Register (4 Byte)
0x6800002C	Codec Initialize Register (4 Byte)
0x68000030	RS323 Data Register (4 Byte)
0x6800003C	RS232 Control Register (4 Byte)
0x68000040 ~ 0x6BFFFFFFF	Reserved(64M – 20 Bytes)
0x6C000000 ~ 0x6FFFFFFF	EMIFB CE3 (64M Bytes)

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0x70000000 ~ 0x7FFFFFFF	Reserved (256M Bytes)
0x80000000 ~ 0x81FFFFFF	SDRAM (32M byte)
0x82000000 ~ 0x8FFFFFFF	Reserved
0x90000000 ~ 0x903FFFFF	EMIFA CE1
0x90400000 ~ 0x9FFFFFFF	Reserved
0xA0000000 ~ 0xA03FFFFF	EMIFA CE2
0xA0400000 ~ 0xAFFFFFFF	Reserved
0xB0000000 ~ 0xB03FFFFF	EMIFA CE3
0xB0400000 ~ 0xBFFFFFFF	Reserved