

DSP STAR
TFT LCD Video Daughtercard
(VM3224K2)
User's Manual
Revision 1.1

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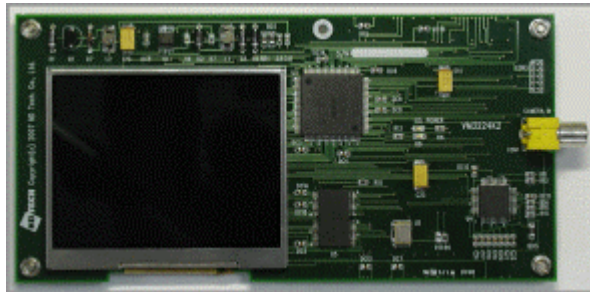
1. TFT LCD Video Daughtercard

The DSP STAR TFT LCD Video Daughtercard (VM3224K2) is a video in/out hardware module, which provides developers with an easy-to-use, cost-effective way to evaluate and develop video processing algorithm based on TMS320C6000™ DSP. The VM3224K2 acquires NTSC/PAL analog video signal and displays digital video data on TFT LCD display. This product is a plug-in for the Texas Instrument's DSK. Since the VM3224K2 complies to TI DSK standard daughtercard interface, the product is compatible with TI Starter Kit, DSP STAR Kit and Third Part EVM board.

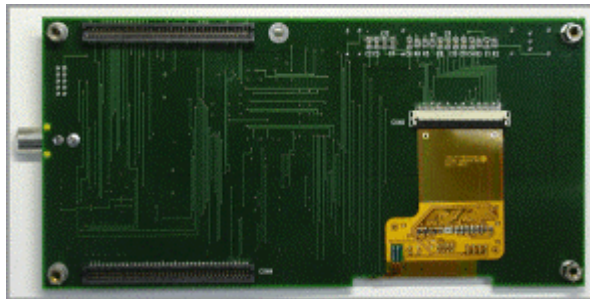
Main features are as follows:

- ✧ Input: NTSC/PAL 30/25 fps
- ✧ Display: 3.5 inch TFT LCD Display
- ✧ Resolution: 320x240 16 bits/pixel
- ✧ Pixel Arrangement: Landscape

Real images of the VM3224K2 are shown below:



(a) Front



(b) Rear

Figure 1. Real Image of TFT LCD Video Module

2. Installation

Figure 2 shows an example of using the VM3224K2 module with DSK.

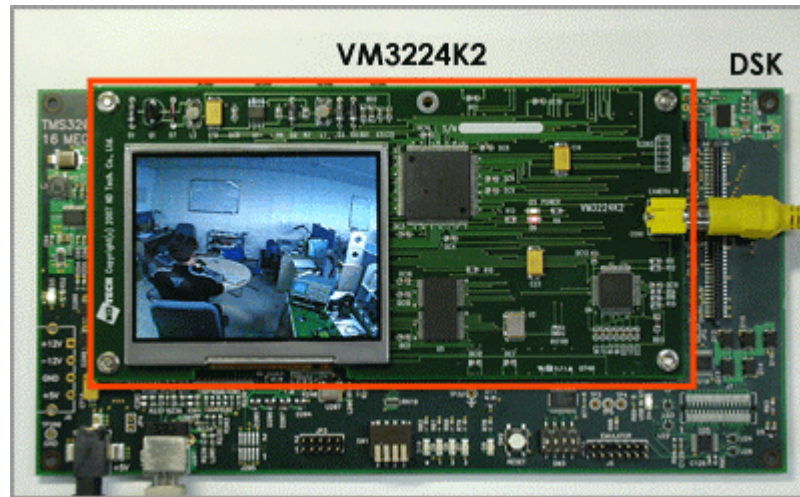


Figure 2. VM3224K2 with DSK

3. Connection Interface

The video module connector is 2 mm pitch connector. Table 1 and Table 2 are the detailed pin descriptions of the connectors.

Table 1. Connector Pinout

Connector 1 (CON4)				Connector 2 (CON3)			
Pin No.	Pin Name	Pin Name	Pin No.	Pin No.	Pin Name	Pin Name	Pin No.
1			2	1	5V	5V	2
3	GND	GND	4	3			4
5	5V	5V	6	5			6
7	GND	GND	8	7			8
9	5V	5V	10	9			10
11			12	11	GND	GND	12
13			14	13			14
15			16	15			16
17			18	17			18
19	3.3V	3.3V	20	19			20
21			22	21	5V	5V	22
23			24	23	A5	A4	24
25	GND	GND	26	25	A3	A2	26
27			28	27			28
29			30	29			30
31	GND	GND	32	31	GND	GND	32
33			34	33			34
35			36	35			36
37	GND	GND	38	37			38
39			40	39			40
41			42	41	3.3V	3.3V	42
43	GND	GND	44	43			44
45			46	45			46
47			48	47			48
49			50	49			50
51	GND	GND	52	51	GND	GND	52
53			54	53	D15	D14	54
55			56	55	D13	D12	56
57			58	57	D11	D10	58
59			60	59	D9	D8	60
61	GND	GND	62	61	GND	GND	62
63			64	63	D7	D6	64
65			66	65	D5	D4	66
67		/INT	68	67	D3	D2	68
69			70	69	D1	D0	70
71			72	71	GND	GND	72
73			74	73	/RE	/WE	74
75	GND	GND	76	75			76
77	GND		78	77		/CE	78
79	GND	GND	80	79	GND	GND	80

Table 2. Pin Descriptions of CON3, CON4

Pin Name	I/O	Description
D[15..0]	I/O	Data Bus
A[5..2]	I	Address Bus
/CE	I	Chip Enable
/RE	I	Read Enable
/WE	I	Write Enable
/INT7	O	Interrupt
3.3V		3.3 V
5V		5V
GND		Ground

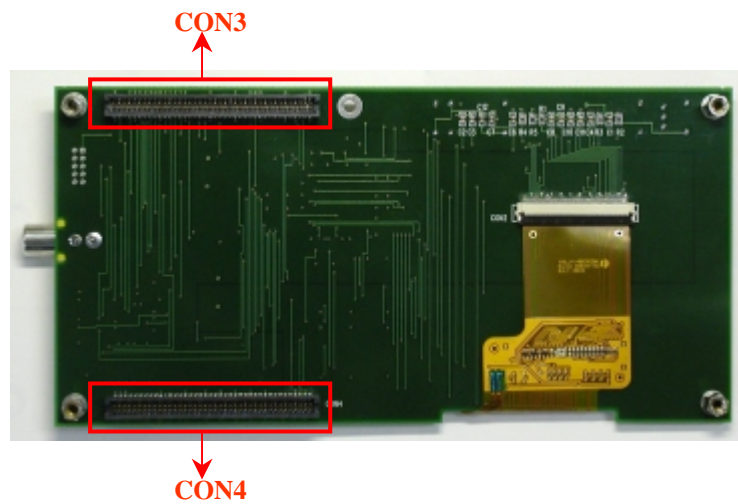


Figure 3. Physical Locations of CON3, CON4

4. Camera Input

Analog video signals are processed on a Philips SAA7113 video decoder to provide YUV 4:2:2 format data for one screen made of 320x240 pixels. The NTSC/PAL camera input signals of the video module are structured as in Figure 4.

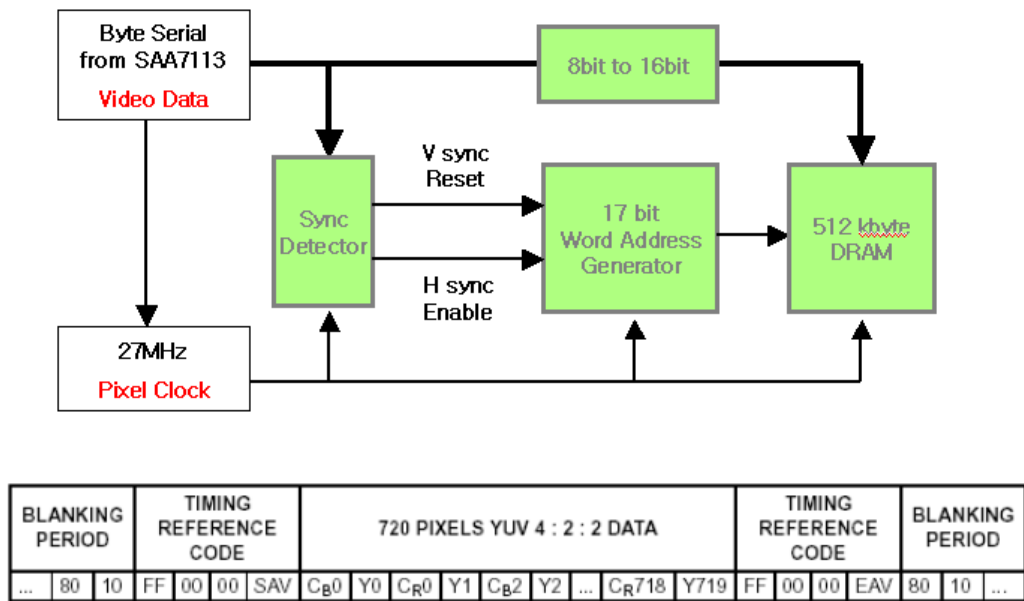


Figure 4. The NTSC Camera Input Structure

Figure 4 shows the process for acquiring digital image data from the camera and storing the acquired data in the 512Kbyte DRAM. Data entering from the SAA7113 appears in sequence as 0x80 → 0x10 → 0xFF → 0x00 → 0x00 → SAV → C_{B0} → Y₀ → C_{R0} → ... → C_{R718} → Y₇₁₉ → 0xFF → 0x00 → 0x00 → EAV → 0x80 → 0x10, as shown at the bottom of Figure 4. The sync detector detects the SAV or the EAV that appears immediately after 0xFF → 0x00 → 0x00, and generates the V and H sync signals to the 18-bit address generator. These two sync signals become the basis for generating address signals, forming a screen size by 320x240, and storing image data in the 512Kbyte DRAM. The data stored in DRAM is structured as the same as in Table 3. The first data indicates (Y₀, U₀) and the second data indicates (Y₁, V₀). Here, Y_i represents the luminance component of *i*th pixel, and U_j and V_j represent the

chrominance components of j th and $(j+1)$ th pixels. Therefore, the 0^{th} pixel is determined by the two byte of data 0 and the low byte of data 1, while the 1^{st} pixel is determined by the low byte of data 0 and the two byte of data 1. In Figure 4, C_B is the U component and C_R is the V component.

Table 3. Data Structure in Screen Buffer

Screen Buffer Address	High Byte	Low Byte
0	Y0	U0
1	Y1	V0
2	Y2	U2
3	Y3	V2
4	Y4	U4
5	Y5	V4

5. TFT LCD Output

The TFT LCD display of the video module is shown schematically in Figure 5. The LCD panel uses an RGB565 pixel expression that is 320x240 in size. The LCD panel must provide pixel data periodically according to the pixel array pattern. Hence, the video module contains memory that can store 320x240 pixel data. The module also contains an LCD controller that conveys memory data to the LCD panel in synchronization with the horizontal and vertical sync signals. The LCD controller generates signals to drive the LCD, and the 18-bit address generator generates pixel data addresses directed to the LCD. Note that the 512 Kbyte DRAM is shared with the camera input, each of which uses 256 Kbytes of DRAM. Thus, the DSP stores image data in the RGB565 format, in order to display it on the TFT LCD.

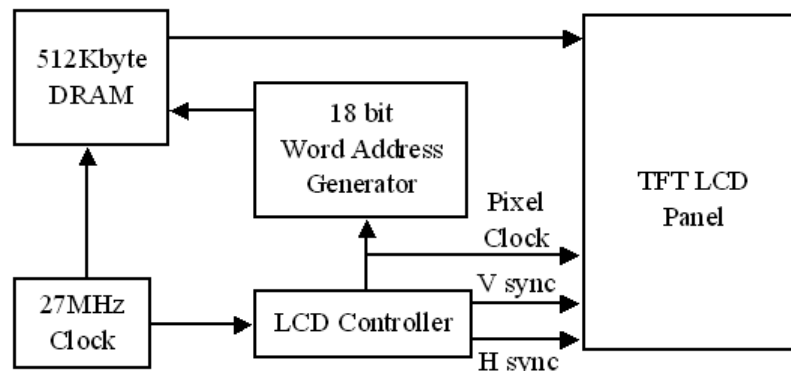


Figure 5. Structure of the TFT LCD Display

Pixel locations in TFT-LCD display are as shown in Figure 6 and Figure 7 depending on panel types. The first number in parenthesis represents the horizontal coordinate on the LCD panel, while the second represents the vertical coordinate. According to the pixel arrangements, the LCD panel is divided into landscape and portrait panels.

(319,0)	(318,0)	...	(1,0)	(0,0)
(319,1)	(318,1)	...	(1,1)	(0,1)
...
(319,238)	(318,238)	...	(1,238)	(0,238)
(319,239)	(318,239)	...	(1,239)	(0,239)

Figure 6. Pixel Locations for the Portrait Panel

(0,0)	(1,0)	...	(318,0)	(319,0)
(0,1)	(1,1)	...	(318,1)	(319,1)
...
(0,238)	(1,238)	...	(318,238)	(319,238)
(0,239)	(1,239)	...	(318,239)	(319,239)

Figure 7. Pixel Locations for the Landscape Panel

When the DSP stores the desired image data in the memory of the video module, the memory location determines the pixel location in the LCD panel. Figure 8 and Figure 9 represent relationships between memory locations and pixel array locations.

Word Address	Decimal Address	Memory	Panel Location
0x00000	0	RGB565	(0,0)
0x00001	1	RGB565	(0,1)
...
0x000ef	239	RGB565	(0,239)
0x000f0	240	RGB565	(1,0)
...
0x001df	479	RGB565	(1,239)
...
0x12b10	76560	RGB565	(319,0)
...
0x12bfe	76798	RGB565	(319,238)
0x12bff	76799	RGB565	(319,239)

Figure 8. Pixel Location and Memory Address for the Portrait Panel

Word Address	Decimal Address	Memory	Panel Location
0x00000	0	RGB565	(0,0)
0x00001	1	RGB565	(1,0)
...
0x0013f	319	RGB565	(319,0)
0x00140	320	RGB565	(0,1)
...
0x0027f	639	RGB565	(319,1)
...
0x12ac0	76480	RGB565	(0,239)
...
0x12bfe	76798	RGB565	(318,239)
0x12bff	76799	RGB565	(319,239)

Figure 9. Pixel Locations and Memory Addresses for the Landscape Panel

6. Control/Status Register

There are four CPLD registers for control and data processing of the video module. Table 4 shows the names and addresses of these four registers and Table 5 shows bit definition of the CNTL register.

The RATE field of CNTL register determines an image capture speed of NTSC/PAL camera input, so the speed is 0 fps for RATE=0, 7.5/6.25 fps for RATE=1, 15/12.5 fps for RATE=2, 30/25 fps for RATE=3. The images obtained from NTSC/PAL camera are then stored in screen buffer. Since the field IE is an interrupt enable bit, the IE=1 generates interrupt with the speed determined from RATE. The interrupt generated in this case is an external interrupt 7 (EXT_INT7). The field RESET is used to initialize the module, so RESET=1 resets the module and RESET=0 makes the module operate normally. The field BL adjusts the back light intensity of the module. When BL=0, the backlight is turned off; when BL=15, light intensity is most intensified.

When the CNTL register is read, previously stored values are read from all the other bits except bit 2 and bit 1, while I2C input data is read from bit 2 and a busy status of the module is read from bit 1.

Table 4. Four Registers for the VM3224K2

DSP Address	Register Name	Description
UIOBASE ¹ +0x00000000	CNTL	Control/Status Register
UIOBASE+0x00000004	DATA	Data Register
UIOBASE+0x00000008	ADDL	Low Address Register
UIOBASE+0x0000000C	ADDH	High Address Register

Table 5. Control/Status Register (CNTL) of the VM3224K2

Bit #	Register Name	Description
15..12	BL	LCD Back Light
11..6	Reserved	Not Used
5..4	RATE	Frame Rate
3	SCL	I2C Clock
2	SDA	I2C Data
1	IE	Interrupt Enable
0	RESET	Reset (active high)

Screen buffer enclosed in the VM3224K2 takes 512K bytes in size. Half of these (256K bytes) are used for the input buffer and the other half (256K bytes) is used for the output buffer. The DSP

¹ UIOBASE = CE2BASE+0x00200000 for C67x or ACE2BASE+0x00000000 for C64x

processor accesses the screen buffer through ADDH and ADDL registers. Therefore, the screen buffer data can be read by putting the data address in ADDH and ADDL registers and then reading it from the DATA register. At this time, the address register value increments automatically. When DSP puts the value on the ADDH register, the ADDL register value automatically becomes zero.

7. Example Programs

Example projects included in the product CD are as follows:

Table 6. Example Programs in product CD

Folder Name	Description
Ball1	Animation of Ball1 moving around TFT LCD display
Ball2	Similar to Ball1 folder, but ball moves faster
Cam2lcd1	Continuous capturing of video signals from NTSC camera and stores in DSP memory
Cam2lcd2	Loopback of video signals from NTSC camera to TFT LCD
ColorBar5	Display of eight vertical color bars in TFT LCD