DSP STAR Camera Module User's Manual

Revision 1.4

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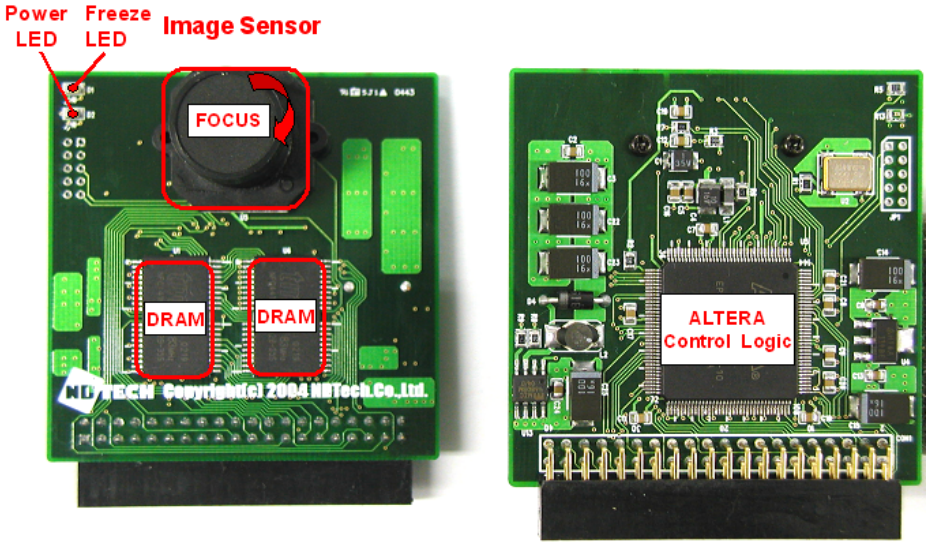
1. DSP STAR Camera Module

1.1 Product Overview

DSP STAR Camera Module VM480 shown in Figure 1 is an image capturing board which is added to DSP STAR Personal hardware board through the expansion port connector. The VM480 houses a CCD camera sensor, through which 30 Hz color signal with 640x480 image resolution is entered as 8-bit byte serial data in YCrCb 4:2:2 format. DSP obtains color image data from the VM480 through bus interface. Capturing image can be upto 640 (H) x 480 (V) pixels in size and upto 30 frames can be processed per second. Embedded FIFO logic allows image capturing very simple and convenient.

As shown in the front view, CCD sensor focus can be adjusted by turning it clockwise or counter clockwise.



(a) front (a) rear

Figure 1. DSP STAR Camera Module

The VM480 product contents are as follows:

- Camera Module Hardware
- Product CD (Reference design also included)

1.2 Hardware Installation

As shown in Figure 2, the Camera Module VM480 is a plug-in module added to the expansion port of the underlying DSP STAR personal hardware. It does not need a separate power since it takes 5 volt power from the expansion connector. When placing the camera module into the expansion port, make sure that the camera directs outward as shown in Figure 2.

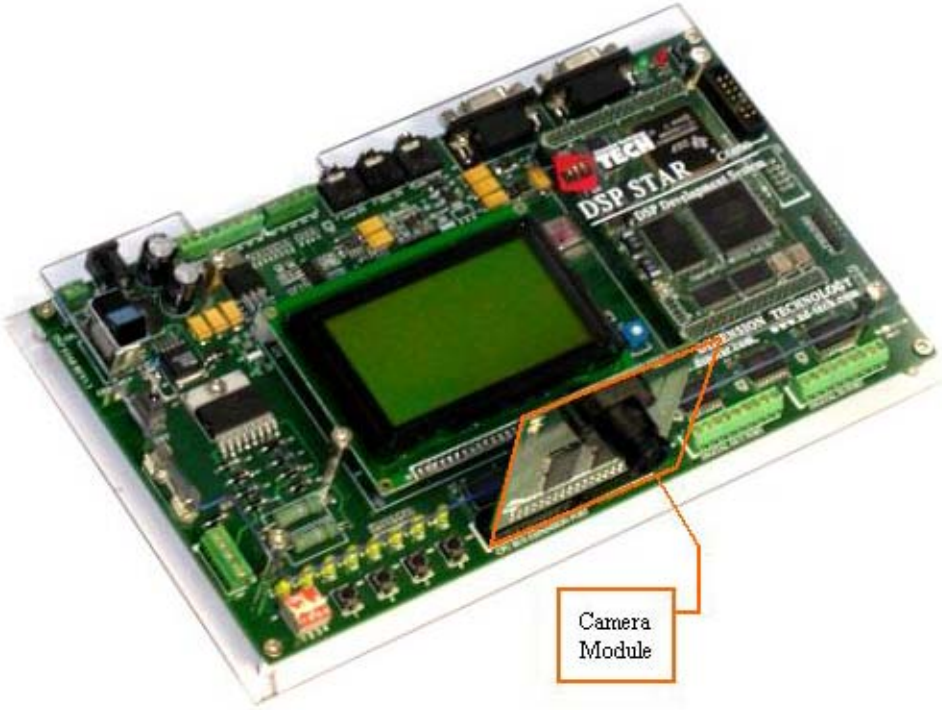


Figure 2. Installation of VM480 into Expansion Connector

The VM480 can also be used with DSP STAR Processor Module as shown in Figure 3.

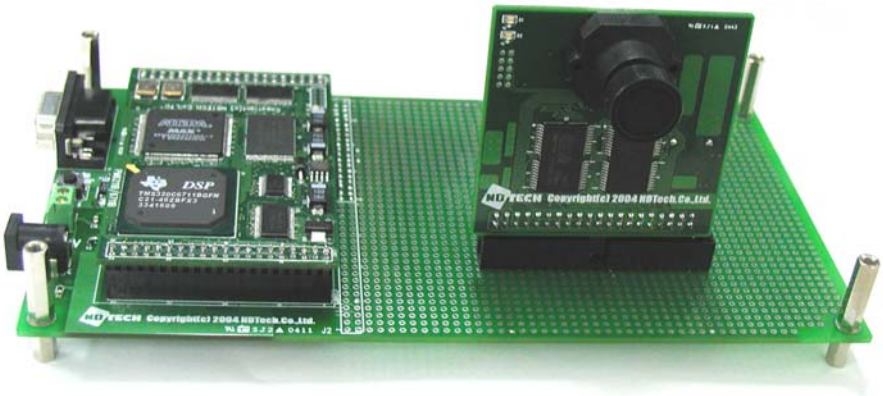


Figure 3. Installation of VM480 with Processor Module

Signals in the expansion connector listed in Table 1 include address bus, data bus, chip enable, read enable, write enable, 5V and so on. Descriptions of these signals are presented in Table 2.

Table 1. CPU Expansion Port Signals

Pin No	Pin Name	Pin No	Pin Name
1	VCC	2	GND
3	CD0	4	CD1
5	CD2	6	CD3
7	CD4	8	CD5
9	CD6	10	CD7
11	CD8	12	CD9
13	CD10	14	CD11
15	CD12	16	CD13
17	CD14	18	CD15
19	CA0	20	CA1
21	CA2	22	CA3
23	CA4	24	CA5
25	CA6	26	CA7
27	CA8	28	CA9
29	CA10	30	CA11
31	CA12	32	CA13
33	CA14	34	CA15
35	INT	36	/URE
37	/UCE	38	/UWE
39	GND	40	VCC

Table 2. Signal Descriptions

Pin Name	Description
VCC	VCC (5V)
GND	Ground
CD[15..0]	Data Bus
CA[15..0]	Address Bus
/UCE	Chip Select Signal
/URE	Read Enable
/UWE	Write Enable
INT	Interrupt

1.3 Hardware Logic

In the hardware logic, one screen of image (one snapshot caputed from image sensor) is represented with 640(W)x480(H) pixels. And these data fed from a camera image sensor is continuously generated at speed of 30Hz. The camera sensor OV7640 of OMNIVISION TECHNOLOGIES INC. is used in the camera module, which can provide various data format such as 60 Hz YCrCb 4:2:2, RGB 4:2:2, RGB raw data 8 bit format, and etc. However, the VM480 supports only YCrCb 4:2:2 8 bit mode.

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The resulting 30Hz video data is cyclically stored in memory contained in the VM480 hardware board. This memory called a screen buffer holds data in pattern as in Table 3. The first word data represents (*Y0*, *U0*) and the second word data represents (*Y1*, *V0*). Here, *Yi* is a luminance component of a *i*th pixel, while *Uj* and *Vj* are two chrominance components of the *j*th and (*j+1*)th pixel. So, the 0th pixel is determined from two-byte data of word 0 and one lower byte data of word 1, while the first pixel is determined from one lower byte of word 0 and two byte data of word 1. In this way, storing one image made of 640 by 480 in pixel size requires a memory of 614400 (=640x480x2) bytes. Hardware logic of the VM480 includes two DRAM, which provides 1M byte memory space. Only upper part of 61440 bytes is utilized as screen buffer with remaining part being unused.

Table 3. Data Structure in Screen Buffer

Screen Buffer Word Address	**High Byte**	**Low Byte**
0	Y0	U0
1	Y1	V0
2	Y2	U2
3	Y3	V2
4	Y4	U4
5	Y5	V4

1.4 Getting Video Data from DSP

The VM480 hardware includes four control registers through which DSP controls the VM480 hardware module and reads screen buffer data. Table 4 shows an address map of these four control registers for TMS320C6713 DSP and Table 5 shows bit definitions of a control/status register. Bit 6 and 7 of the control register is SIZE, which determins an image resolution. For different values of SIZE=0, 1, 2, and 3, the screen resolution is 80x60, 160x120, 320x240 and 640x480 pixels, respectively. The field RATE at bit 4 and 5 determines a screen capture speed. For RATE=0, 1, 2, and 3, frame speeds are 0, 7.5, 15, and 30 frames per second, respectively. The field IE is an interrupt enable bit and generates interrupt every 1/(frame speed) second at value of 1. The interrupt created here is an external interrupt 7. The RESET field is used to initialize a camera sensor. When RESET=1, the sensor is at reset and ready for normal operation.

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Table 4. Four Registers for the Camera Module

DSP Address	RS1	RS0	Register Name	Description
0x90320000	0	0	CNTL	Control/Status Register
0x90320004	0	1	DATA	Data Register
0x90320008	1	0	ADDL	Low Address Register
0x9032000c	1	1	ADDH	High Address Register

Table 5. Bit Definition for Control/Status Register (CNTL)

Bit Number	Register Name	Description
15..8	Reserved	not used
7..6	SIZE	Frame Size
5..4	RATE	Frame Rate
3	SCL	I2C Clock
2	SDA	I2C Data
1	IE	Interrupt Enable
0	RESET	Reset(active high)

Since the screen buffer consists of 1Mbytes, 19-bit word address is needed for access to screen buffer. So, in order to facilitate DSP's access to the screen buffer, two address register is contained in the camera module. These registers are ADDH and ADDL as in Table 4. When DSP enters address information in these two address registers, it can read data from the screen buffer through the Data register. After data read, the address registers are automatically increased. When DSP sets a value to ADDH, the value of ADDL becomes zero. So, in order to read one frame, DSP should enter 0 in ADDH and read the Data Register as many times as the number of pixels for one screen.

1.5 Example Program

Figure 1 shows a Code Builder Image View through which image data of YUV format in size 320x240 acquired from the camera sensor is displayed.

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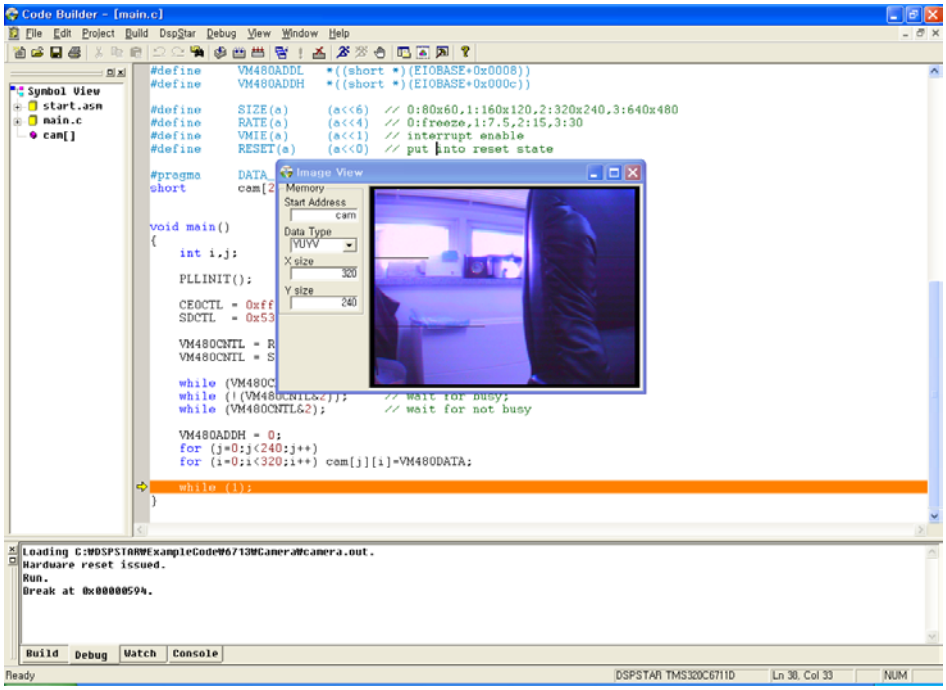

Figure 1. Image Data acquired from the Camera Module (320x240)

The list of example programs included in the product CD is as follows:

Table 6. List of Example Programs

Example Projects	Descriptions
colorbar	Vertical Color Bar
historgram	Histogram Computation
vmodule	Image Capture from Image Sensor
yuv2rgb	YUV->RGB Conversion
yuv2u	Extraction of indivual y, u, v components from composite YUV signal

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